CLAIMS

What is claimed is:

1. A method of detecting shorts between first and second sets of interconnect lines in a device, the method comprising:

driving the first and second sets of interconnect lines to a first logic level;

measuring a reference current IDDQref with the first and second sets of interconnect lines at the first logic level;

driving the first set of interconnect lines to the first logic level and the second set of interconnect lines to a second logic level different from the first logic level;

measuring a total leakage current IDDQtot with the first set of interconnect lines at the first logic level and the second set of interconnect lines at the second logic level;

determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref;

rejecting the device if the IDDQsig exceeds a predetermined threshold; and

passing the device if the IDDQsig does not exceed the predetermined threshold.

2. The method of Claim 1, wherein the first logic level is power high and the second logic level is ground.

3. The method of Claim 1, wherein the device is a programmable logic device (PLD).

4. The method of Claim 3, wherein:

driving the first and second sets of interconnect lines to a first logic level comprises configuring the PLD with a first configuration bitstream; and

driving the first set of interconnect lines to the first logic level and the second set of interconnect lines to a second logic level comprises configuring the PLD with a second configuration bitstream.

5. The method of Claim 3, wherein the PLD is a field programmable gate array (FPGA).

6. The method of Claim 3, wherein the PLD is partially defective.

7. The method of Claim 3, wherein:

the first set of interconnect lines comprises interconnect lines unused in a PLD design targeted to the PLD; and

the second set of interconnect lines comprises interconnect lines used in the PLD design.

8. The method of Claim 7, wherein the unused interconnect lines are driven to the first logic level by default.

9. The method of Claim 1, wherein the first and second sets of interconnect lines comprise sets of alternating interconnect lines within a group of physically adjacent interconnect lines in the device.

10. The method of Claim 1, wherein the steps of the method are performed in the order shown.

11. A method of detecting shorts between used and unused interconnect lines in a design targeted to a programmable logic device (PLD), the method comprising:

configuring the PLD with both used and unused interconnect lines being driven to a first logic level, the used interconnect lines being interconnect lines in the PLD

used in the design and the unused interconnect lines being interconnect lines in the PLD not used by the design;

measuring a reference current IDDQref with both used and unused interconnect lines at the first logic level;

configuring the PLD with the used interconnect lines being driven to a second logic level different from the first logic level and the unused interconnect lines being driven to the first logic level;

measuring a total current IDDQtot with the used interconnect lines at the second logic level and the unused interconnect lines at the first logic level;

determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref;

rejecting the PLD for the design if the IDDQsig exceeds a predetermined threshold; and

passing the PLD for the design if the IDDQsig does not exceed the predetermined threshold.

12. The method of Claim 11, wherein the used interconnect lines comprise a subset of interconnect lines in the PLD that are utilized by the design.

13. The method of Claim 11, wherein the first logic level is power high and the second logic level is ground.

14. The method of Claim 11, wherein the PLD is a field programmable gate array (FPGA).

15. The method of Claim 11, wherein the PLD is partially defective.

16. The method of Claim 11, wherein the unused interconnect lines are driven to the first logic level by default.

17. The method of Claim 11, wherein the steps of the method are performed in the order shown.

18. A computer-readable storage medium comprising computer-executable code for detecting shorts between first and second sets of interconnect lines in a device, the medium comprising:

code for driving the first and second sets of interconnect lines to a first logic level;

code for driving the first set of interconnect lines to the first logic level and the second set of interconnect lines to a second logic level different from the first logic level;

code for measuring a reference current IDDQref with the first and second sets of interconnect lines at the first logic level, and measuring a total leakage current IDDQtot with the first set of interconnect lines at the first logic level and the second set of interconnect lines at the second logic level;

code for determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref; and

code for rejecting the device if the IDDQsig exceeds a predetermined threshold, and passing the device if the IDDQsig does not exceed the predetermined threshold.

19. The computer-readable storage medium of Claim 18, wherein:

the device is a programmable logic device (PLD);

the code for driving the first and second sets of interconnect lines to a first logic level comprises a first configuration bitstream for the PLD; and

the code for driving the first set of interconnect lines to the first logic level and the second set of interconnect lines to a second logic level comprises a second configuration bitstream for the PLD.

20. The computer-readable storage medium of Claim 18, wherein the first and second sets of interconnect lines comprise sets of alternating interconnect lines within a group of physically adjacent interconnect lines in the device.

21. A computer-readable storage medium comprising computer-executable code for detecting shorts between used and unused interconnect lines in a design targeted to a programmable logic device (PLD), the medium comprising:

code for configuring the PLD with both used and unused interconnect lines being driven to a first logic level, the used interconnect lines being interconnect lines in the PLD used in the design and the unused interconnect lines being interconnect lines in the PLD not used by the design;

code for configuring the PLD with the used interconnect lines being driven to a second logic level different from the first logic level and the unused interconnect lines being driven to the first logic level;

code for measuring a reference current IDDQref with both used and unused interconnect lines at the first logic level, and measuring a total current IDDQtot with the used interconnect lines at the second logic level and the unused interconnect lines at the first logic level;

code for determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref; and

code for rejecting the PLD for the design if the IDDQsig exceeds a predetermined threshold, and passing the PLD for the design if the IDDQsig does not exceed the predetermined threshold.

22. A computer system for detecting shorts between first and second sets of interconnect lines in a device, the computer system comprising:

a first driving module for driving the first and second sets of interconnect lines to a first logic level;

a second driving module for driving the first set of interconnect lines to the first logic level and driving the second set of interconnect lines to a second logic level different from the first logic level;

a current measuring module for measuring a reference current IDDQref with the first and second sets of interconnect lines at the first logic level, and for measuring a total leakage current IDDQtot with the first set of interconnect lines at the first logic level and the second set of interconnect lines at the second logic level;

a signature current determining module for determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref; and

an evaluation module for rejecting the device if the IDDQsig exceeds a predetermined threshold and passing the device if the IDDQsig does not exceed the predetermined threshold.

23. The computer system of Claim 22, wherein:

the device is a programmable logic device (PLD);

the first driving module comprises a first configuration bitstream for the PLD; and

the second driving module comprises a second configuration bitstream for the PLD.

24. The computer system of Claim 22, wherein the first and second sets of interconnect lines comprise sets of alternating interconnect lines within a group of physically adjacent interconnect lines in the device.

25. A computer system for detecting shorts between used and unused interconnect lines in a design targeted to a programmable logic device (PLD), the computer system comprising:

a first configuring module for configuring the PLD with both used and unused interconnect lines being driven to a first logic level, the used interconnect lines being interconnect lines in the PLD used in the design and the unused interconnect lines being interconnect lines in the PLD not used by the design;

a second configuring module for configuring the PLD with the used interconnect lines being driven to a second logic level different from the first logic level and the unused interconnect lines being driven to the first logic level;

a current measuring module for measuring a reference current IDDQref with the used and unused interconnect lines at the first logic level, and measuring a total current IDDQtot with the unused interconnect lines at the first logic level and the used interconnect lines at the second logic level;

a signature current determining module for determining a signature current IDDQsig equal to a difference between the IDDQtot and the IDDQref; and

an evaluation module for rejecting the PLD for the design if the IDDQsig exceeds a predetermined threshold, and passing the PLD for the design if the IDDQsig does not exceed the predetermined threshold.